

The rejection included in the June 29 Office Action constitutes a new ground of rejection that is not necessitated by Applicants' April 11, 2005 Amendment. Thus, the finality of the rejection must be withdrawn.

Turning to the contents of the June 29 Office Action, claims 1-14 were rejected under 35 U.S.C. 112, first paragraph, for allegedly failing the written description requirement. Specifically, the rejection took issue with the language: "N low-bandwidth data sources, M low-bandwidth data destinations, M/N ingress multiplexers, and M/N egress multiplexers," asserting that support for that language was not found in this specification or drawings as originally filed. Applicants traverse the rejection because support is found in the application, as explained herein.

Referring to the PCT publication WO-A-00/38376 which is the application on which the present US application is based, on page 1, in the last paragraph there is reference to "N low-bandwidth data sources and M low-bandwidth output data sources." Thus, the first of the features that the Office Action objected to is clearly supported by the application as originally filed.

Moreover, there is a statement at line 5 of page 6 of the PCT application that states:

"the central interconnect has M/N high-bandwidth ports." Further, referring to the last paragraph on page 1 of the present application's specification, the specification teaches "there is provided a scheduling and arbitration process for use in a digital data switching arrangement of the type in which a central switch under the direction of a master control provides the cross-connections between a number of high-bandwidth ports to which are connected on the ingress side of the central switch a number of ingress multiplexers, *one for each high-bandwidth input port* and on the egress side a number of egress multiplexers, *one for each high-bandwidth output port*."

In other words, the present application's specification clearly teaches that there are M/N high-bandwidth ports and also that, for each high-bandwidth port, there is an ingress multiplexer and an egress multiplexer. Therefore, the features of claim 1 that there are M/N ingress multiplexers and M/N egress multiplexers is clearly supported by the application as filed.

Furthermore, on a basic level, it must be pointed out that there are N input ports and M virtual output queues per ingress multiplexer (see, e.g., the Abstract). Since the number of virtual output queues is, by definition, equal to the number of low-bandwidth output ports (destination) in the switch and there are N (low-bandwidth) input ports per multiplexer, there must be M/N multiplexers in the switch.

Moreover, Applicants' Figure 1 illustrates N as equal to 2 and M as equal to 6. The low-bandwidth input ports are numbered 4 and the low-bandwidth output ports are numbered 5. There are two low-bandwidth input ports per ingress multiplexer (numbered 2) and there are six low-bandwidth output ports in total.

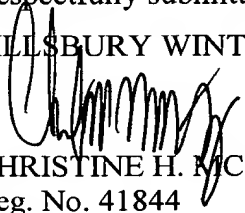
Furthermore, although the ingress and egress multiplexers are drawn as separate components in Figure 1, as stated at the top of page 3, "in practice, a switch is required to support full-duplex ports, such that an ingress multiplexer and its corresponding demultiplexer may be considered a single full-duplex device." Thus, the application's specification clearly supports the features of current claim 1, e.g., that there are N low-bandwidth data sources, M low-bandwidth data destinations, M/N ingress multiplexers and M/N egress multiplexers. Therefore, the rejection is traversed.

Based on the foregoing remarks, Applicants submit that the pending claims are allowable. Applicants request allowance of the application with these claims. However, if the Examiner feels there is anything further necessary to place this application in condition for allowance, Applicants request the Examiner to telephone Applicants' undersigned representative at the number below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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